Large-Signal Relaxation-Time Model for HEMTs and MESFETs

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Abstract — A nonquasi-static charge-conserving spline-based model has been implemented in the EEsof harmonic-balance simulator. The model uses a relaxation-time approximation to describe the intrinsic charging dynamics of unipolar transistors under arbitrary excitation. On-wafer large-signal measurements of HEMTs closely match simulation results.

Introduction

The increasing call for circuits operating in the millimeter-wave regime, the expanding role of the HEMT at these higher frequencies, and the push to demonstrate first-pass MMIC design capability have created the need for large-signal nonquasi-static models suitable for HEMTs as well as MESFETs. In response, various workers [1-3] have abandoned the use of inflexible polynomial representations of FETs and turned to spline interpolation of parameters calculated from measured small-signal data. Others [3-5] have introduced intrinsic delays into charge-conserving models so as to improve accuracy at the higher frequencies. Because of its speed, the harmonic balance technique has gained popularity for analyzing RF circuits consisting of both linear and nonlinear components. To our knowledge, no one has yet demonstrated a spline-based nonquasi-static (i.e. intrinsic-delay-representing) large-signal model compatible with commercial harmonic balance simulators. This paper presents the formulation, implementation, and experimental verification of such a model.

Model Theory and Implementation

The nonquasi-static formulation presented here follows a charge-relaxation-time approach proposed by Ward [6] in lieu of the formulation shared by references [3-5]. The relaxation-time approximation has been successfully applied to other physical problems (e.g. the solution of the Boltzmann Transport Equation) where stimulus history must be considered when calculating far-from-steady-state behavior. This approach is both intuitive and compatible with commercial simulators.

A symbolic depiction of the intrinsic model is given in Fig. 1. The source and drain charges represent the instantaneous state of the channel under both steady-state and far-from-steady-state conditions. The variation of at least two independent charge variables must be considered to account for

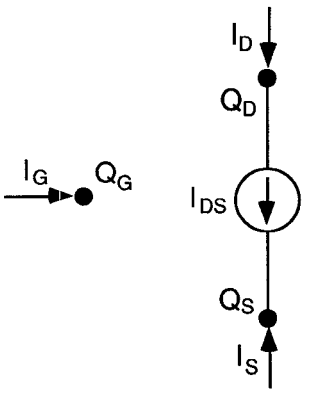

Fig. 1 Symbolic representation of intrinsic (bias-dependent) portion of the large-signal model.

the two independent displacement currents possible with a three terminal device. For slowly varying terminal voltages, these charges keep pace with their steady-state values, $Q_S^{ss}(V_{gs}, V_{ds})$ and $Q_D^{ss}(V_{gs}, V_{ds})$, which are represented by spline surfaces. Since bias-dependent capacitances are not independently specified, charge conservation is strictly enforced. In the case of higher frequencies or more abrupt excitations, channel charge cannot respond instantaneously. Therefore, Q_S and Q_D are allowed to relax toward their (time-varying) steady state values. The differential equations which describe this behavior are of the form:

$$\frac{dQ_S}{dt} = -\frac{\Delta Q_S}{\tau_S} = -\frac{Q_S - Q_S^{ss}(V_{gs}, V_{ds})}{\tau_S(Q_S+Q_D, V_{ds})}. \qquad (1)$$

This describes the large-signal behavior of the displacement currents. The particle current, I_{DS}, flowing between the drain and source charge pools depends on the instantaneous charge

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available for conduction, $Q_S + Q_D$, and the source-drain voltage. Therefore, it too is delayed with respect to the value demanded by the terminal voltages. Note also that the time constants are also functions of the channel state. The external terminal currents can be calculated by applying current continuity to each pool. The resulting model self-consistently describes the small-signal, large-signal, and transient behavior of FETs.

An exact equivalent circuit representation for the model described by (1) is shown in Fig. 2 and has been implemented in

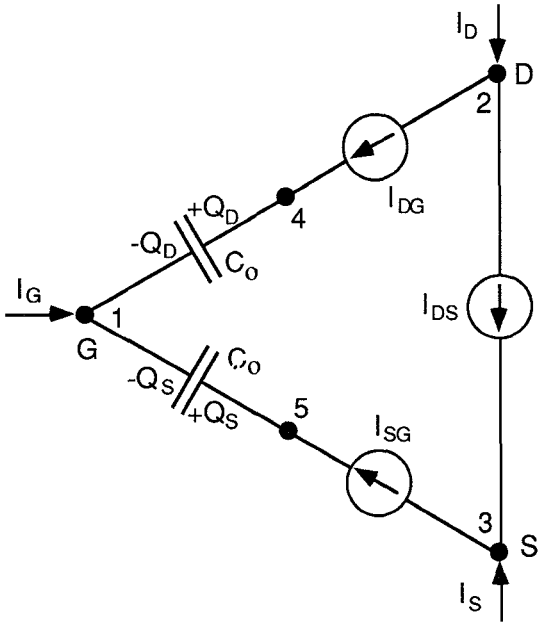

Fig. 2 Exact circuit representation of the differential equations describing the relaxation-time model. Two fixed capacitors (of arbitrary value) and three voltage-controlled current sources are required.

a popular commercial harmonic balance simulator (EEsof LIBRA). User provided subroutines calculate the displacement currents from the steady state and instantaneous charges. For the case of the source branch,

$$I_{SG} \equiv \frac{dQ_S}{dt} = -\frac{C_o \cdot (V_5 - V_1) - Q_S^{ss}(V_{gs}, V_{ds})}{\tau_S(C_o \cdot (V_4 + V_5 - 2V_1), V_{ds})}. \qquad (2)$$

The fixed capacitors accommodate the source and drain charges while making their instantaneous values accessible to the user subroutines via voltages $V_5 - V_1$ and $V_4 - V_1$ respectively. Aside from questions of matrix conditioning, their value, C_o, is arbitrary. This formulation has two advantages. First, only the present node voltages, not their time derivatives or past values, are required to calculate the nonquasi-static currents. Second, the CAD simulator assumes responsibility for maintaining model state variables Q_S and Q_D via the simulator state variables V_5 and V_4. These charges (or linearly related voltages) serve as a concise representation of the device's departure from steady state due to its stimulus history. This circuit representation is compatible with any simulator accepting user provided subroutines because it does not require communication of voltage derivatives, time, time increments, or state variables other than the customary node voltages.

To verify the above circuit implementation, the governing differential equations were also solved by direct integration in the time domain. For all circuit topologies, frequencies, biases, and drive levels tested, exact agreement was observed between waveforms calculated by direct integration and the LIBRA implementation. Insensitivity to the value for C_o was also confirmed via this approach.

Large-Signal On-Wafer Measurement Technique

One difficulty in making on-wafer microwave measurements is the need to separate and measure the incident and reflected signals close to the device under test (DUT). Small-signal S-parameter test sets use directional couplers for signal separation which, for ease of commercial packaging, are many wavelengths from an on-wafer DUT. Elaborate error correction routines have been studied and developed by the microwave industry to account, in the frequency domain, for these and other uncertainties [7]. To make accurate nonlinear large-signal on-wafer measurements, one needs to minimize these errors by separating the signals as closely as possible to the DUT and employing analogous correction procedures over the spectrum of generated harmonics [8].

To achieve this, directional couplers (reflectometers) from 2 to 18 GHz were mounted on a probe station in a manner similar to the mounting of the input tuner required by on-wafer noise systems [9]. The RF coupled incident and reflected signals were measured with a Microwave Transition Analyzer (MTA) by using a time-shift sampling technique (HP 70820A). Fig. 3 shows a block diagram of the measurement setup. The MTA

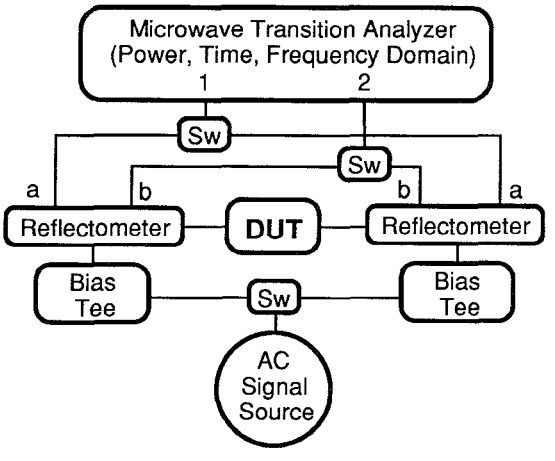

Fig. 3 Block diagram of equipment used for large signal measurements.

allows simultaneous observation and measurement of time and frequency domain signals. Error corrected measurements to the probe tips are obtained by using an external controller, RF switches, and traditional small-signal error correction techniques (TRL) with the MTA [10]. Alternatively, a first-order scalar correction is possible using the user-correction routines of the MTA. The latter approach was used for the power measurements presented here. The output was terminated in 50 Ω for all measured data presented in this paper.

Comparison of Measurement and Simulation

To verify the model, bias-dependent DC and small-signal S-parameter measurements of 1×100 μm^2 coplanar AlGaAs/GaInAs HEMTs were performed on-wafer. The large gate length was chosen to make the peak current-gain cutoff frequency (23 GHz) close to the bandwidth of the large-signal measurement equipment and allow testing of the model where intrinsic delays would be more significant. Bias-independent series parasitics were determined using an RF end-resistance technique [11]. Inter-pad parasitic capacitances were derived from measurements of a gateless FET on insulating GaAs. With this information, S-parameters were converted to intrinsic admittance parameters for the transistor [11]. Bias-dependent partial derivatives of charge and current were calculated directly from the intrinsic admittance parameters. Subsequently, bias-dependent relaxation-time constants were determined via an optimization procedure [12].

Using model parameters extracted from the small-signal data, tensor-product cubic splines were calculated for current, charge, and delay surfaces. Several aspects of this process merit elaboration. First, spline creation was performed using approximation rather than interpolation algorithms to avoid spurious ripples introduced by measurement uncertainty. Second, physically motivated constraints were imposed during spline fitting to insure realistic behavior despite measurement uncertainty. For example, the constraint $\partial I_{DS}/\partial V_{gs} \geq 0$ (after accounting for gate current) prevents ripples near pinchoff that might disrupt simulation of class B amplifier circuits. Third, integration of partial derivative data was not performed prior to spline fitting since such an approach would rely on a limited number of integration paths. Rather, spline coefficients were optimized to minimize derivative error directly. In the case of I_{DS}, DC data was fit concurrently with RF partial-derivative data. Fourth, visual inspection of the fit quality and final adjustment of spline knot points was performed in an interactive spline and graphics environment. Using a method to be reported elsewhere [12], a change of variables was effected to introduce the charge dependence of the current and delay splines.

Spline surfaces were linked to the harmonic balance simulator via user provided subroutines. The previously measured bias-independent parasitic elements were reassembled around the intrinsic FET and harmonic balance simulations performed for direct comparison against measured large-signal data. In addition to the parasitic elements, the simulation circuit included two gate diodes with saturation current and ideality factors determined by DC measurement and confirmed by RF characterization. Finally, simple circuit representations of the bias-tees were included for completeness.

Large-signal harmonic output power vs. available input power was measured on-wafer using the MTA. Fig. 4 compares measured and simulated P_{out} (fundamental, second, third, and fourth harmonic) vs. P_{in} data for the unmatched HEMT at three different bias conditions. The threshold voltage is –0.2 V. The fundamental frequency is 4 GHz to allow harmonics to fall within the directional-coupler bandwidth. Agreement between measured and simulated fundamental powers is better than 1 dB except in deep saturation where power reversal is underestimated. The number of minima in the measured harmonic powers were correctly predicted and their position matched to within 3 dB input power. The generally excellent agreement is a consequence of both the spline approach and the use of nonconstant delays.

Conclusion

A charge-relaxation-time model has been successfully implemented in an off-the-shelf commercial simulator and shows excellent agreement with large-signal measurements. By describing the variation of instantaneous charges as a relaxation toward the time-varying steady-state target set by terminal bias, nonquasi-static behavior is accurately represented. Small-signal measurements were used to calculate the steady-state charges, currents, and time constants used in the simulation. Because these parameters are represented by bivariate splines, the characteristics of diverse transistors, including HEMTs and MESFETs [12] have been accurately modeled.

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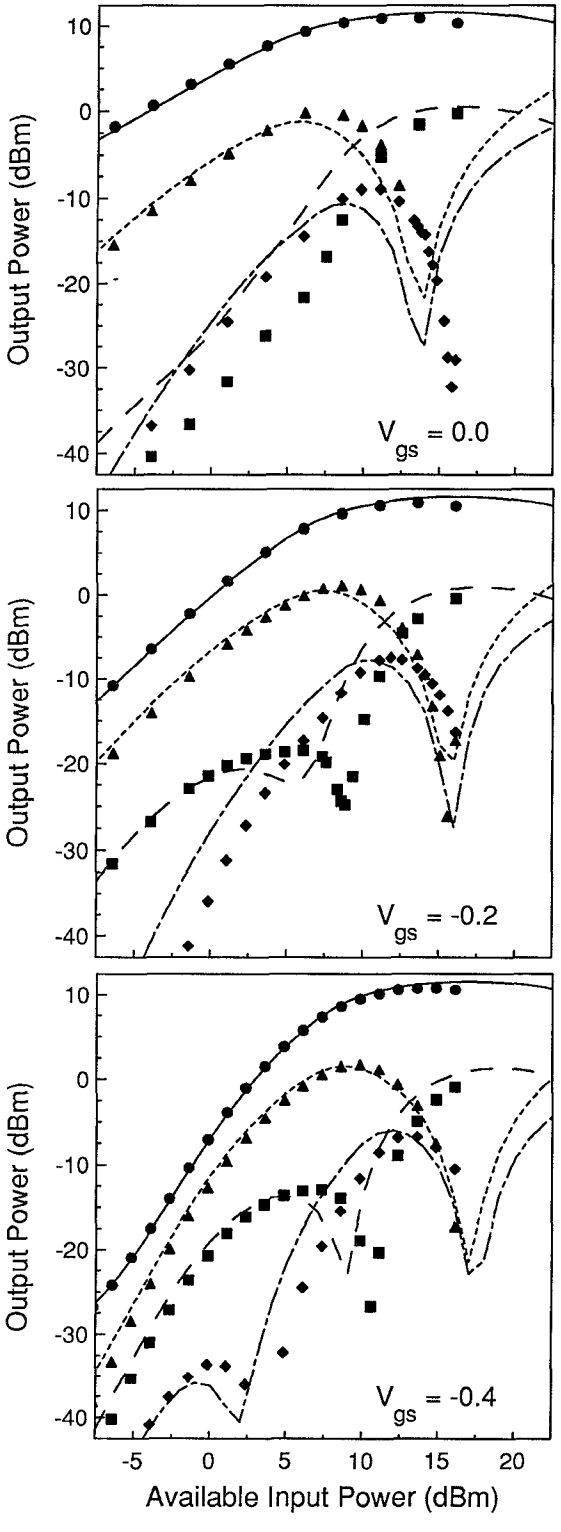

Fig. 4 Comparison of simulated output power for fundamental, 2nd, 3rd, and 4th harmonic powers (——— , - - - - - , — — , and —— · —— respectively) with measured powers (●, ▲, ■, and ◆ respectively). V_{ds} = 2.5 volts. The input frequency is 4 GHz.

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